SIMULATION AND EXPERIMENTAL RESULTS OF SOURCE HARMONIC TUNING ON LINEARITY OF POWER GaAs FET UNDER CLASS AB OPERATION

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ABSTRACT

Nonlinearity of GaAs FET amplifiers under class AB operation such as abrupt increase of the output power against the input power can be effectively reduced by suppressing even-order harmonic distortion in gate RF voltage. In this paper, we demonstrate the effect of the source harmonic tuning and condition for improving the linearity of power GaAs FET's under class AB operation by the source harmonic tuning technique.

INTRODUCTION

Recent microwave power amplifiers especially for advanced telecommunication systems application are often designed to operate GaAs FET's under class AB condition for having high efficiency [1], [2]. Properly designed amplifiers have exhibited excellent performance; however, class AB amplifiers sometimes have some problems.

An example of measured output power P_{out}, drain current I_{ds}, and gate current I_g against input power P_{in} under $I_{dss}/4$ (class AB) conditions is shown in Fig. 1, where I_{dss} denotes the saturated drain current. The device being measured is an internally matched power GaAs FET, in which a JS8820-AS was used. The measurement was carried out at 5.9 GHz. Due to lower bias current the output power begins to be off from linear operation at lower input power, and as the input power increases, however, output power rapidly increase up to saturation. This kind of transfer characteristic quite differs from the usual one, and thereby this might cause some problems in system insertion.

Particularly for internally matched power GaAs FET's, the input and output matching circuits are built in the packages, and designers of power amplifiers thus are not able to manipulate the matching condition. Moreover, many internally matched power FET's are usually designed to be operated in class A; therefore the FET's are not driven in the optimum circuit condition under class AB operation.

On improvement of efficiency in power amplifiers, a harmonic reaction microwave amplifier has been proposed [3], and the design method and performances have been demonstrated [3], [4]. However, they have shown the optimum design parameters only for the output matching conditions, and much attention has not been paid for the conditions of the input matching circuits. On the other hand, a source harmonic controlled circuit has been proposed [5], and it has shown the harmonic tuning effect on the efficiency under class F or B operation; however, the linearity of a class AB amplifier has not been dis-

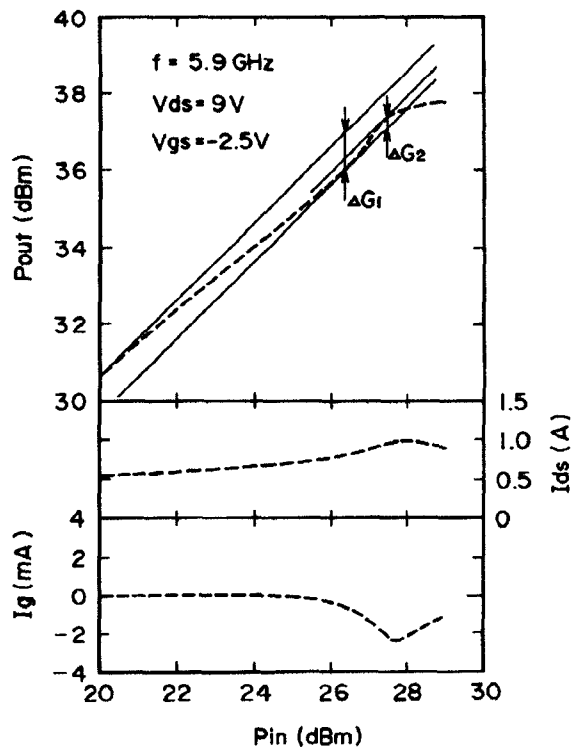

Fig. 1 An example of measured output power P_{out}, drain current I_{ds}, and gate current I_g against input power P_{in} under $I_{dss}/4$ condition.

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cussed yet. While many discussion for improving efficiency of microwave amplifiers by harmonic tuning technique have been made to date, there have been few on the linearization.

In this paper, we demonstrate momentous issues for distortion in the input circuit of GaAs FET's for class AB operation, and discuss the condition for improving the linearity of amplifiers by source harmonic tuning technique.

Nonlinear Simulation of Power GaAs FET under Class AB Operation

In order to investigate the experimental result, we have performed nonlinear circuit simulation. An equivalent circuit model of a GaAs FET, JS8820-AS, is shown in Fig. 2, where each model parameter description is given in [6] and [7], and the values of the parameters are summarized in Table 1.

To obtain an accurate simulation result for the gate circuit, an improved gate current model [7] shown in Fig. 3 was proposed. As shown in Fig. 2, the gate current model is connected between the intrinsic gate and drain, and between gate and source, respectively. In this research, to clarify the essential point at issue, the values of the negligible parasitic elements, L_g, L_d, and C_{ds}, were set

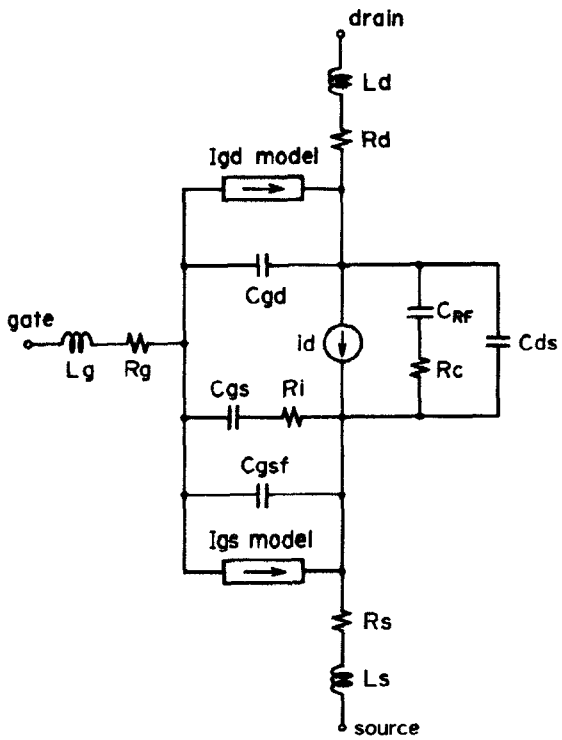

Fig. 2 An equivalent circuit model of GaAs FET.

Table 1 Summary of the model parameter values of JS8820-AS.

Drain Current Parameters (I_{ds})			
β	0.709	α_1	2.22
V_{T0} (V)	-3.33	α_2	0.0
γ	0.025	Q	1.8
λ	-0.016	b	0.22
Capacitance Parameters (C_{gs} and C_{gd})			
C_{gs0} (pF)	14.16	δ	0.2
C_{gd0} (pF)	1.98	V_{max}	0.5
Δ	0.2	Z	0.5
Gate Current Parameters (I_{gs} and I_{gd})			
I_{sfgs} (A)	1.2×10^{-10}	I_{sfgd} (A)	1.2×10^{-10}
I_{sr1gs} (A)	1.0×10^{-8}	I_{sr1gd} (A)	1.0×10^{-8}
I_{sr2gs} (A)	1.0×10^{-8}	I_{sr2gd} (A)	1.0×10^{-8}
n_{fgs}	1.15	n_{fgd}	1.15
n_{r1gs}	40	n_{r1gd}	40
n_{r2gs}	58	n_{r2gd}	60
R_{r1gs}	2.0×10^5	R_{r1gd}	2.0×10^5
Equivalent Circuit Elements			
R_g (Ω)	0.37	C_{gsf} (pF)	0.40
R_s (Ω)	0.15	C_{RF} (nF)	13.2
R_d (Ω)	0.20	C_{ds} (pF)	0.0
R_{in} (Ω)	0.45	L_g (pH)	0.0
R_c (Ω)	12.0	L_s (pH)	8.3
		L_d (pH)	0.0

to be 0. A JS8820-AS exhibits 2.9 A of I_{dss} and -3.4 V of V_T at V_{ds} = 3 V, and a transconductance g_m of 1.1 S at V_{ds} = 9 V and $I_{ds} \cong I_{dss}/2$. It has a breakdown voltage V_{BR} of about 22.5 V. Simulation has been performed with a commercially available harmonic balance circuit simulator.

Simulated results of P_{out}, I_{ds}, and I_g at frequency of 6 GHz under $I_{dss}/4$ are shown as dashed lines (without harmonic tuning) in Fig. 4. The output impedance matching circuit was designed to have a load resistance R_L of 7 Ω which is almost the optimum condition for class A operation, and the input impedance matching circuit was

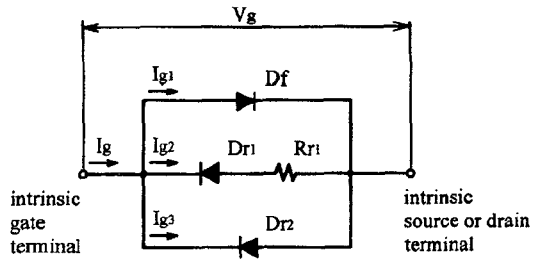

Fig. 3 An improved gate current model for GaAs FET.

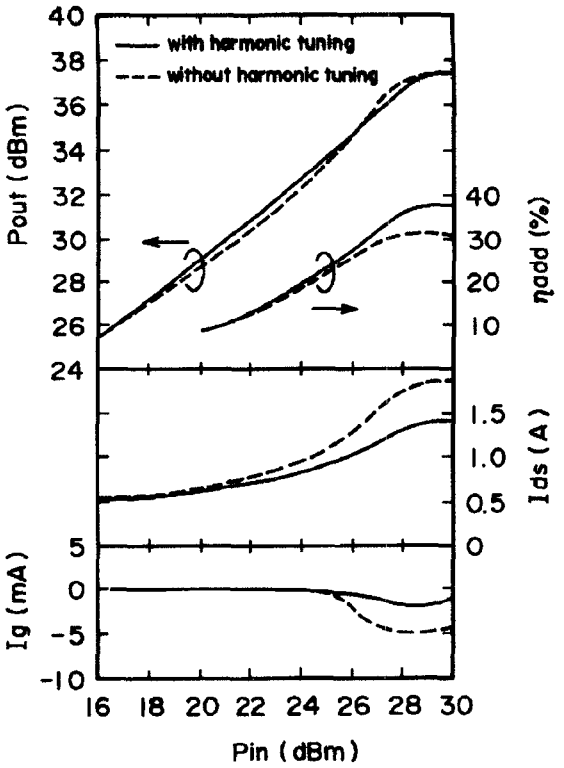

Fig. 4 Simulated results of P_{out}, I_{ds}, and I_g at frequency of 6 GHz under $I_{dss}/4$. Solid and dashed lines are the case for the source circuit with and without harmonic tuning, respectively.

designed to be less than 1.5 of VSWR. The matching networks were determined with low pass configuration. Simulated result shown in Fig. 4 with dashed lines has exhibited a good agreement with measured one shown in Fig. 1.

Effect of Source Harmonic Tuning on Linearity of Power GaAs FET

To see the effect of source harmonic tuning on the linearity of a power GaAs FET, an circuit configuration shown in Fig. 5 has been analyzed, where λ shows wavelength. By using short circuited transmission line with a quarter wavelength at fundamental frequency f_0, even-order harmonics are terminated. To examine the effect of phase of terminating condition, the length θ of a transmission line connected between the gate and the short circuited transmission line has been varied in nonlinear simulation. In order to simplify analysis, the characteristic impedance's of the transmission lines have assumed to be 50 Ω.

Phase plane trajectories of time-dependent instant gate current i_g versus gate-to-source voltage v_{gs} are shown

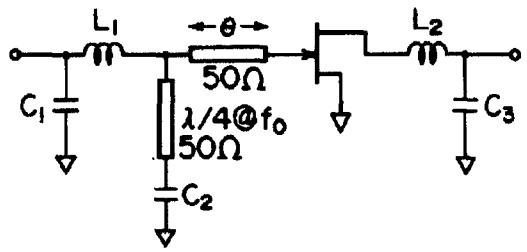

Fig. 5 Circuit configuration of source harmonic tuning by using short terminated transmission line with a quarter wavelength for fundamental frequency f_0.

in Fig. 6. The lines show for P_{in} = 16 dBm and 28 dBm. For P_{in} = 28 dBm, we show three simulated results; the cases of with harmonic tuning of $\Gamma_S = 1.0 \angle 180°$ for $2f_0$, without harmonic tuning, and without harmonic tuning when $V_{BR} \to \infty$. When $V_{BR} \to \infty$, v_{gs} reaches about -12 V, and time-dependent instant gate-to-drain voltage v_{gd} extends more than -30 V correspondingly. Consequently, v_{gd} exceeds V_{BR}, and gate-to-drain breakdown current thus flows. This growth of v_{gs} in the region $v_{gs} < V_T$ seems to be one of the parametric effects produced by the nonlinearity of the gate-to-source capacitance C_{gs}, and the effect must be unavoidable for GaAs FET's. When the source harmonic tuning is employed, this extension of v_{gs} is effectively reduced by suppressing even-order harmonics as shown in Fig. 6.

Simulated results of P_{out}, I_{ds}, and I_g when the source harmonic tuning circuit of $\Gamma_S = 1.0 \angle 180°$ for $2f_0$ is employed are shown as solid lines (with harmonic tuning) in Fig. 4. Comparing with the case for without harmonic tuning (dashed lines), linearity is greatly improved, and increase of drain current and gate current are also reduced. Then, a power added efficiency η_{add} is enhanced, too, as shown in Fig. 4.

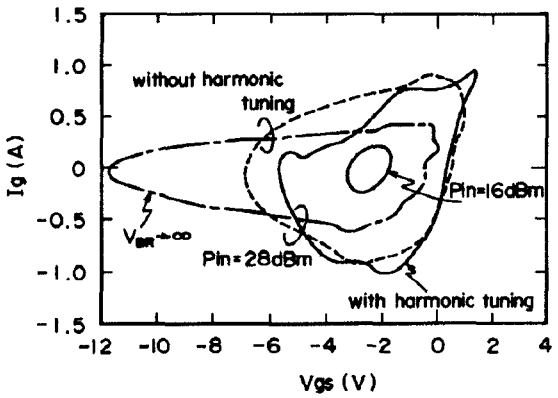

Fig. 6 Phase plane trajectories of gate current versus gate-to-source voltage.

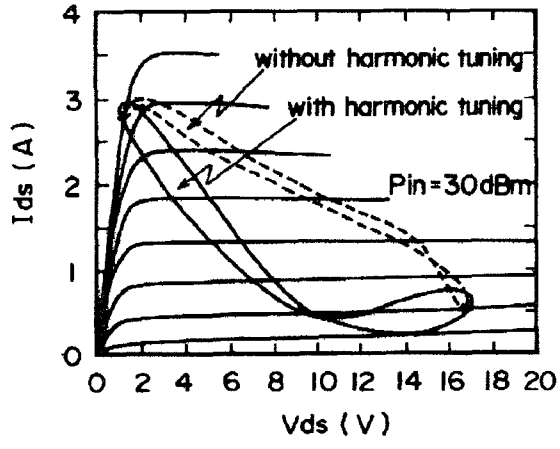

Fig. 7 Phase plane trajectories of drain current versus drain voltage.

Phase plane trajectories of time-dependent instant drain current i_{ds} versus drain voltage v_{ds} at P_{in} = 30 dBm shown in Fig. 7 clearly exhibit the effectiveness of the source harmonic tuning. In Fig. 7, the solid line show the case when the source harmonic tuning is employed and the dashed line for without harmonic tuning. Without the source harmonic tuning circuit, the trajectory is located far from that at d.c. bias position (V_{ds} = 9 V and V_{gs} = -2.5 V). On the other hand, when the source harmonic tuning circuit of $\Gamma_S = 1.0 \angle 180°$ for $2f_0$ is adopted, the trajectory is kept around the location of d.c. bias.

The dependence of gain variations ΔG_1, ΔG_2 and relative harmonic reduction in v_{gs} on the length θ of a transmission line connected between the gate and the short circuited transmission line is shown in Fig. 8. The definition of ΔG_1 and ΔG_2 are shown in Fig. 1, and θ denotes the electrical length for fundamental frequency.

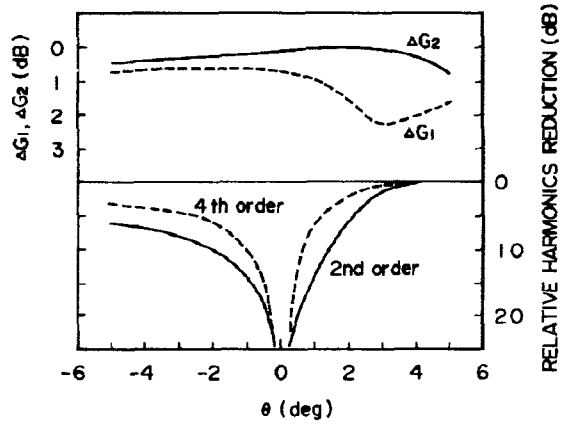

Fig. 8 The dependence on the length θ of a transmission line connected between the gate and the short circuited transmission line

For suppressing the abrupt increase in gain ΔG_2, the harmonic tuning is considered to be effective for $-3° < \theta < 3°$. On the other hand, the gain reduction ΔG_1 is worsened around $\theta = 3°$. Thus, Fig. 8 shows that the optimum condition is to be $\theta = 0°$, and that preferable performance would be given with the condition of $-3° < \theta < 1°$.

Conclusion

The effect of the source harmonic tuning and the condition for improving the linearity of GaAs FET's are demonstrated. The circuit configuration for harmonic tuning is simple, yet easily realizable particularly in monolithic microwave integrated circuit (MMIC) configuration.

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References

[1] K. Mori, M. Nakayama, Y. Itoh, S. Murakami, Y. Nakajima, T. Takagi, and Y. Mitsui, "Direct efficiency and power calculation method and its application to low voltage high efficiency power amplifier," *IEICE Trans. Electron.*, vol. E78-C, no. 9, pp. 1229-1236, Sept. 1995.

[2] A. Sugimura, K. Tateoka, H. Furukawa, and K. Kanazawa, "A high efficiency GaAs power amplifier of 4.6 V operation for 1.5 GHz digital cellular phone systems," *IEICE Trans. Electron.*, vol. E78-C, no. 9, pp. 1237-1240, Sept. 1995.

[3] T. Nojima and S. Nishiki, "High efficiency microwave harmonic reaction amplifier," *1988 IEEE MTT-S Int'l Microwave Symp. Dig.*, pp. 1007-1010.

[4] T. Takagi, Y. Ikeda, Y. Nakajima, and T. Hashimoto, "Design method of high efficiency UHF band monolithic multistage FET amplifier using harmonic terminating technique," *IEICE Trans.*, vol. J76-C-I, no. 11, pp. 389-398, Nov. 1993.

[5] M. Nakayama, M. Maeda, H. Takehara, H. Masato, S. Morimoto, and Y. Ota, "High efficiency linear amplifiers using source second-harmonic control for digital cellular phones," *1995 Asia Pacific Microwave Conference Proc.*, pp. 64-67, Oct. 1995.

[6] J. Onomura, S. Watanabe, and S. Kamihashi, "An accurate FET model for microwave nonlinear circuit simulation," *IEICE Trans. Electron.*, vol. E78-C, no. 9, pp. 1223-1228, Sept. 1995.

[7] S. Watanabe and Y. Oda, "An improved gate current model of GaAs FET's for nonlinear circuit simulation," to be published in *IEICE Trans. Electron.*, vol. E79-C, no. 5, May 1996.